IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application		
Inventor	:	NEGISHI
Application No.	:	10/540,596
Filed	:	06/23/2005
For	:	CIRCUIT ARRANGEMENT

APPEAL BRIEF

On Appeal from Group Art Unit 2116

Date: 07/23/2007

By: Michael Ure
Attorney for Applicant
Registration No. 33,089

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Michael Ure
(Name)

M Ure 7/23/07
(Signature and Date)

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TABLE OF CASES

NONE

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1, 3 and 6-9 are pending, of which claims 1, 3, 6 and 9 stand finally rejected and form the subject matter of the present appeal. Claims 8 and 9 were indicated as containing allowable subject matter. Claims 2, 4 and 5 have been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to a shift register structure that includes a clock control circuit. The control circuit receives a clock signal, a data input signal of a first

stage and a data output of the first stage. The control signal produces a modified clock signal that is applied to a plurality of stages. Depending upon the data sequence applied to the shift register, the modified clock signal may have clock pulses corresponding to clock pulses of the applied clock signal, or may have missing pulses as compared to the applied clock signal. The output of the shift register is identical to a conventional shift register having no control circuit. By conserving clock pulses as allowed by the data sequence, power is conserved.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A device comprising:		
a first delay circuit, a second delay circuit, and a third delay circuit, each for outputting data in response to a pulse of a clock signal, the first, second and third delay circuits being serially coupled;	Fig. 1: F0, F1, F6	Page 4, lines 4-28; page 10, lines 1-11.
a signal processing circuit for processing said outputted data from said first delay circuit; and	Fig. 1, 4; Fig. 6, 4.	Page 10, lines 12-27
a control circuit for controlling whether said second delay circuit and said third delay circuit should be supplied with said pulse of said clock signal on the basis of whether outputted data from said first delay circuit in response to said clock signal is equal to data to be outputted from said first delay circuit in response to the next pulse.	Fig 1, 5; Fig. 6, 5.	Page 10, lines 12-27

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 102(a), claims 1, 3, 6 and 9 are anticipated by Nakao.

VII. ARGUMENT

I. Rejection of Claims 1, 3, 6 and 9 as Anticipated by Nakao

A principal distinction between Nakao and the present invention lies in a manner in which control circuit determines for each stage whether or not a clock signal is to be supplied.

In the case of the present invention, as recited in claim 1, a control circuit controls whether the *second* delay circuit *and* the *third* delay circuit should be supplied with the pulse of the clock signal on the basis of whether outputted data from the *first* delay circuit in response to the clock signal is equal to data to be outputted from the *first* delay circuit in response to the next pulse. Note especially that in Fig. 1 of the present application, the second and third (etc.) delay circuits receive the *identical* clock signal as produced by the control circuit depending on the data sequence applied to the first delay circuit.

In Nakao, the situation is much different. Each delay circuit receives a different clock signal CK1, CK2, CK3, etc. These respective clock signals are produced based on the data input and data output of *that delay circuit*. So the clock signal for the second delay circuit is produced based on the data input and data output of the second delay circuit. The clock signal for the third delay circuit is produced based on the data input and data output of the third delay circuit, etc.

There is no teaching in Nakao of a control circuit that controls whether the *second* delay circuit *and* the *third* delay circuit should be supplied with the pulse of the clock signal on the basis of whether outputted data from the *first* delay circuit in response to the clock signal is equal to data to be outputted from the *first* delay circuit in response to the next pulse.

Accordingly, Nakao does not anticipate the invention of claim 1.

With regard to dependent claims 3, 6 and 9, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claim.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: 7/23/07

By: Michael Urc
Attorney for Applicant
Registration No. 33,089

IX. APPENDIX: THE CLAIMS ON APPEAL

1. A device comprising:

a first delay circuit, a second delay circuit, and a third delay circuit, each for outputting data in response to a pulse of a clock signal, the first, second and third delay circuits being serially coupled;

a signal processing circuit for processing said outputted data from said first delay circuit; and

a control circuit for controlling whether said second delay circuit and said third delay circuit should be supplied with said pulse of said clock signal on the basis of whether outputted data from said first delay circuit in response to said clock signal is equal to data to be outputted from said first delay circuit in response to the next pulse.

3. A circuit device as claimed in claim 2, wherein each of said delay circuits comprises a plurality of data inputting portions for receiving data and a plurality of data outputting portions for outputting data.

6. A circuit device as claimed in claim 1, wherein said control circuit comprises: a deciding circuit for deciding whether said second delay circuit should be supplied with said pulse of said clock signal on the basis of whether said outputted data from said first delay circuit in response to said pulse of said clock signal is equal to said data to be outputted from said first delay circuit in response to the next pulse; and a clock driver for allowing or blocking supply of said pulse of said clock signal to said second delay circuit

in accordance with a decision of said deciding circuit.

9. A circuit device as claimed in claim 1, wherein each of said first delay circuits and second delay circuits is constructed by one or more D flip-flops.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE